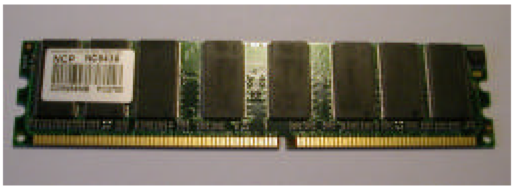
Site WEB

www.rmn.uhp-nancy.fr/Grandclaude/index.html

Chapitre 5 bis

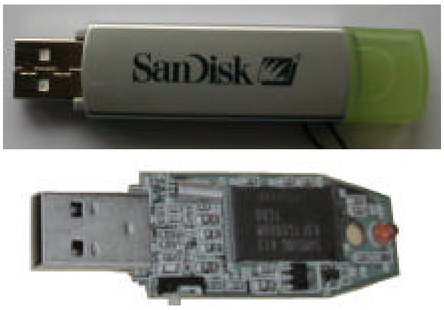
Stockage et transmission de l'information

Stockage de l'information



Mémoire RAM

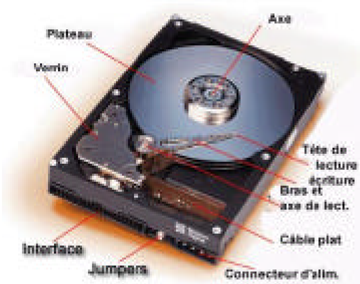
Stockage de l'information



Clef USB

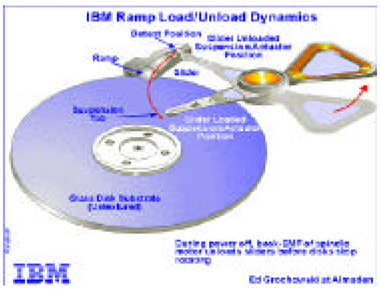
Stockage de l'information

Disque dur



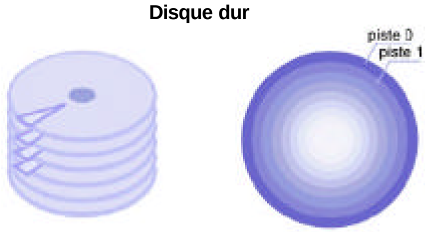
Stockage de l'information

Disque dur



Stockage de l'information

Disque dur

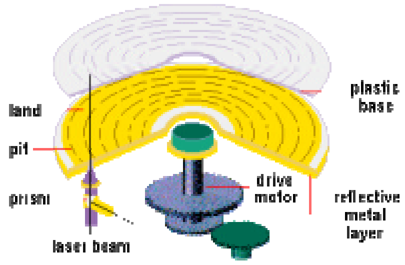


Ecriture : Aimantation du support magnétique

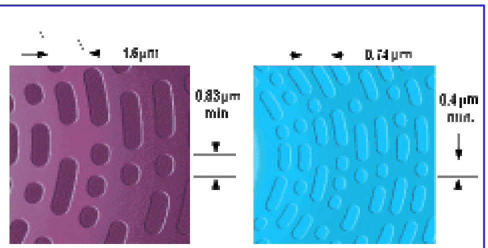
Lecture : Détection du changement d'aimantation

Stockage de l'information

CD-ROM



Stockage de l'information

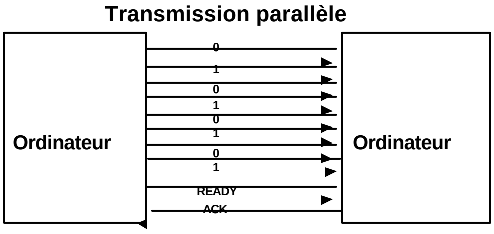


CD-ROM — 650 à 700 Mo

DVD — 4,7 à 9,4 Go

Transmission de l'information

Transmission parallèle

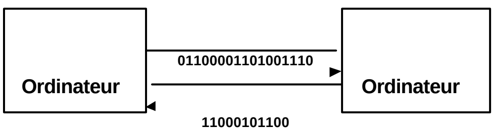


10 fils pour transmettre / 10 fils pour recevoir

ou transmission bidirectionnelle, alternativement

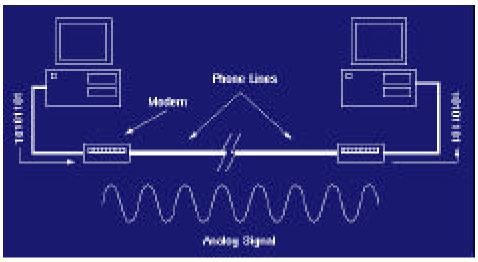
Transmission de l'information

Sérialisation les données

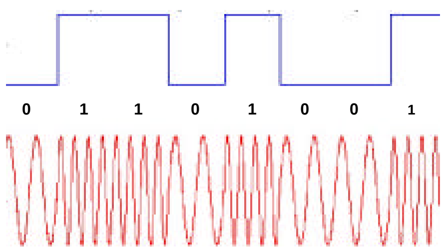


RS232 – Ethernet – Réseaux numériques …

Transmission de l'information



Transmission de l'information

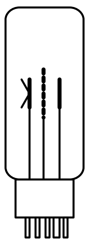


Modem : modulation

Chapitre 6

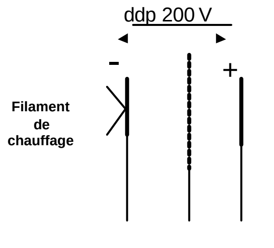
Notions d'électronique numérique

Triode

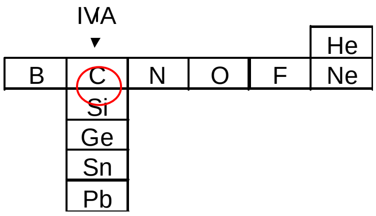


Poids : 100 g
Consommation : 20 W
Volume : 40 cm³

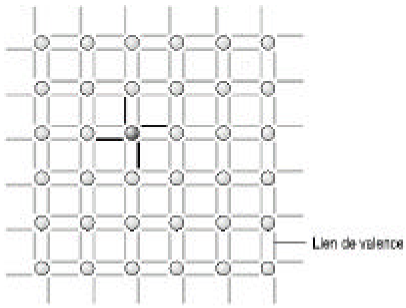
Triode



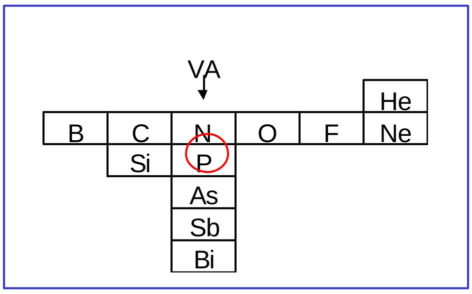
Silicium



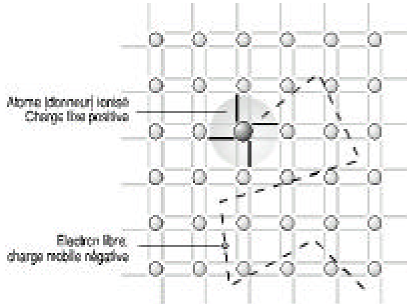
Silicium pur - Isolant



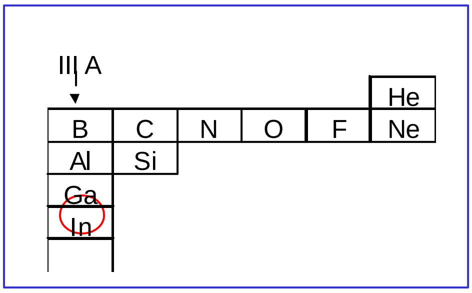
Silicium dopé n



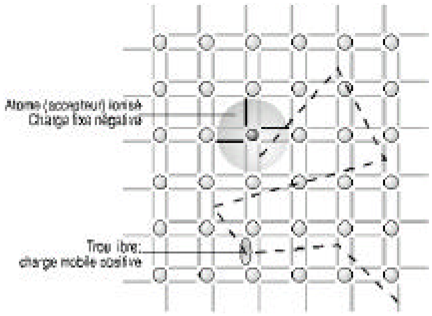
Silicium dopé n



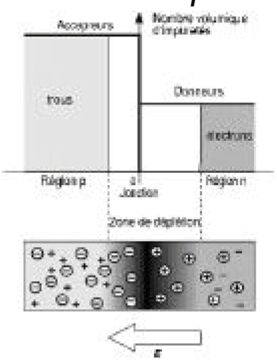
Silicium dopé p



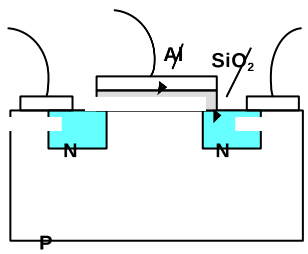
Silicium dopé p



Jonction pn

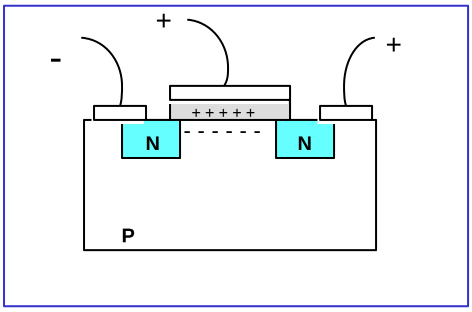


Transistor MOS

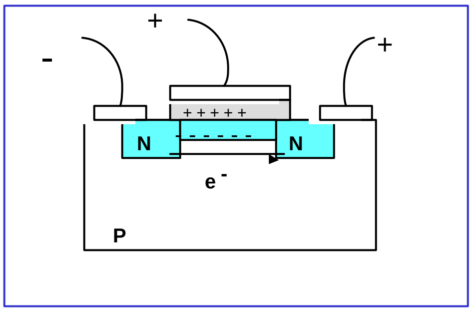


Métal – Oxyde - Silicium

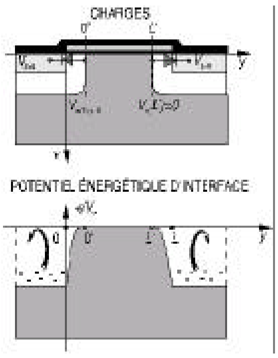
Transistor MOS – Canal N



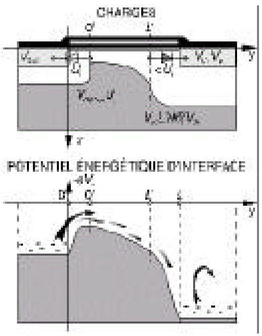
Transistor MOS – Canal N



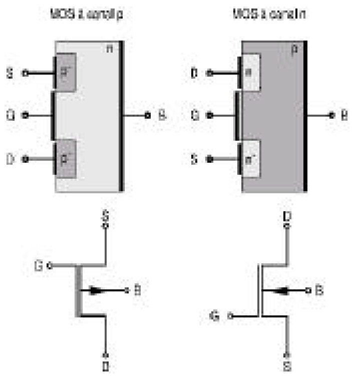
Transistor MOS bloqué (flat band)



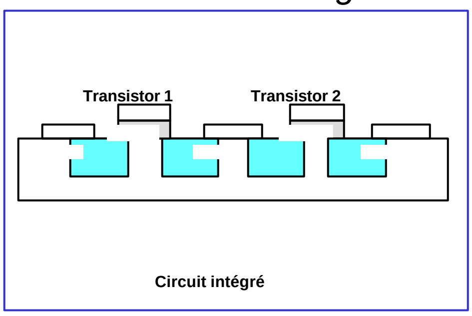
Transistor MOS saturé



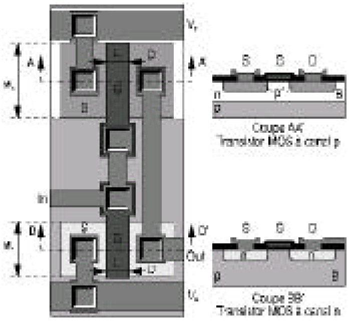
Transistor MOS



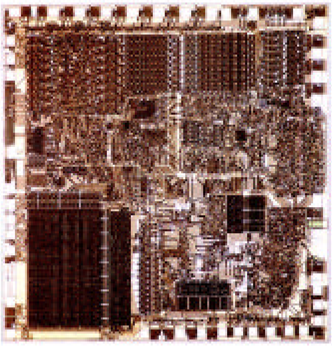
Transistor MOS – Intégration



Transistor MOS – Intégration



Transistor MOS – Intégration



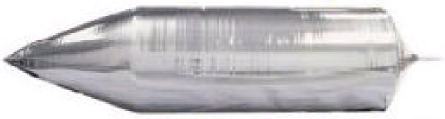
Fabrication du silicium pur

$SiO_2 + 2\ C$ -> $Si + 2\ CO$

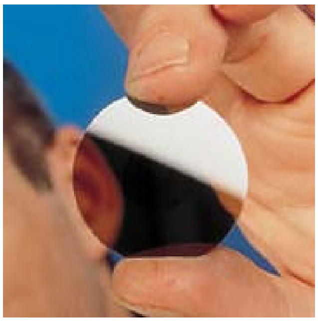
$Si + 2\ Cl_2$ -> $Si\ Cl_4$

$Si\ Cl_4 + 2H_2$ -> $Si_{pur} + 4\ HCL$

Fabrication du silicium pur

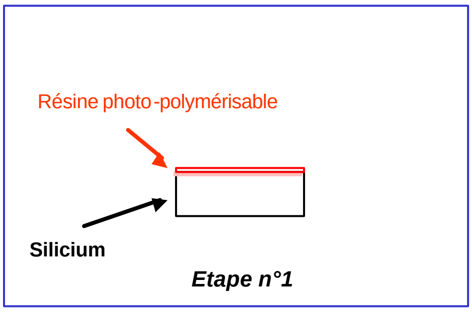


Transistor MOS – Intégration



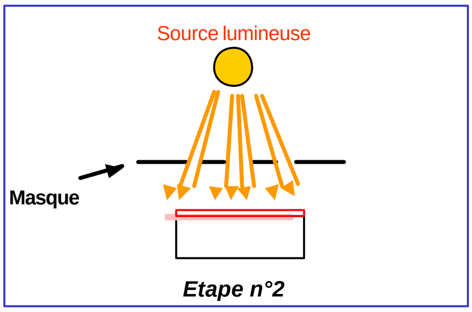
Transistor MOS – Intégration

Transistor MOS – Fabrication



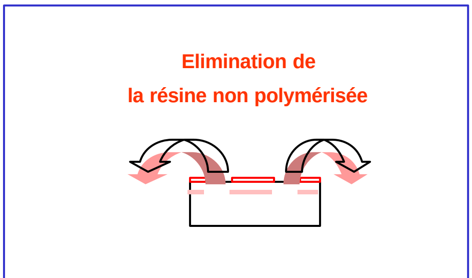
Etape n°1

Transistor MOS – Fabrication



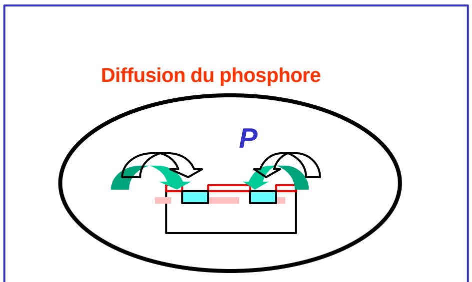
Etape n°2

Transistor MOS – Fabrication



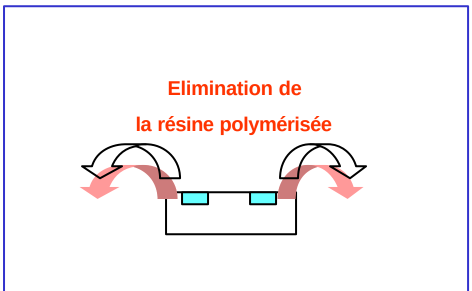
Etape n°3

Transistor MOS – Fabrication



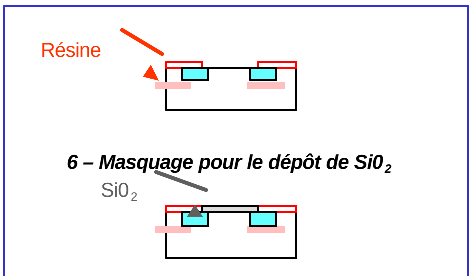
Etape n°4

Transistor MOS – Fabrication



Etape n°5

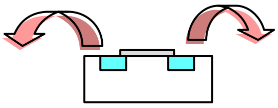
Transistor MOS – Fabrication



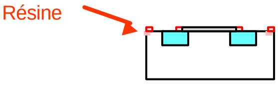
6 – Masquage pour le dépôt de SiO_2

7 – Dépôt de SiO_2

Transistor MOS – Fabrication

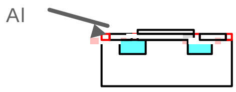


8 – Elimination de la résine polymérisée

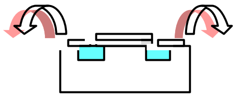


9 – Masquage pour le dépôt d'aluminium

Transistor MOS – Fabrication

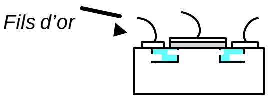


10 – Dépôt d'aluminium



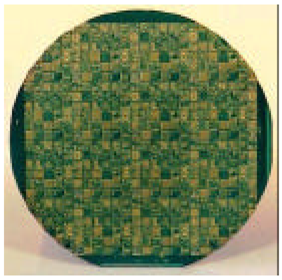
11 – Elimination de la résine polymérisée

Transistor MOS – Fabrication



12 – Soudure des fils d'interconnexion

Circuits intégrés – Fabrication

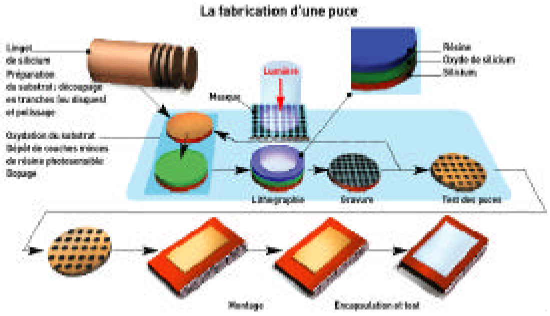


Circuits intégrés – Fabrication

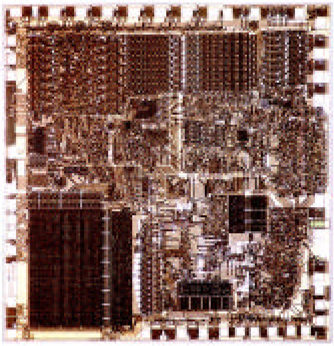
Circuits intégrés – Fabrication

Circuits intégrés – Fabrication

Circuits intégrés – Fabrication



Circuit intégré



Transistor MOS

Utilisation en électronique numérique = Interrupteur

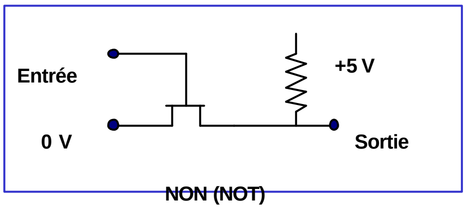
Transistor MOS

Boole + Shannon

–

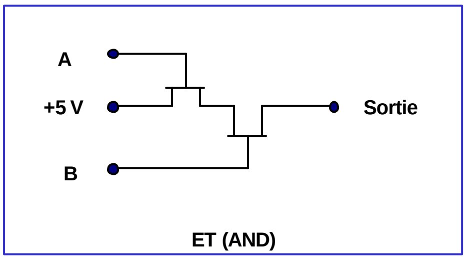
Faire des calculs avec des interrupteurs

Circuit logique NON

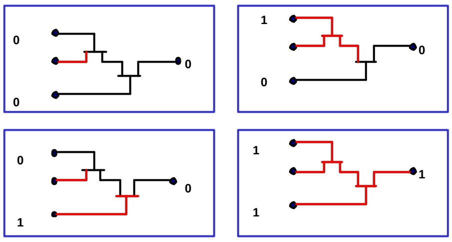


Entrée	Sortie
0	1
1	0

Circuit logique ET

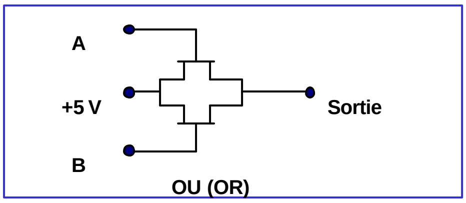


Circuit logique ET



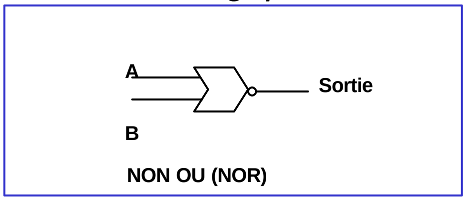
A	B	Sortie
0	0	0
	1	0
1	0	0
	1	1

Circuits logiques



A	B	Sortie
0	0	0
	1	1
1	0	1
	1	1

Circuits logiques



A	B	Sortie
0	0	1
	1	0
1	0	0
	1	0

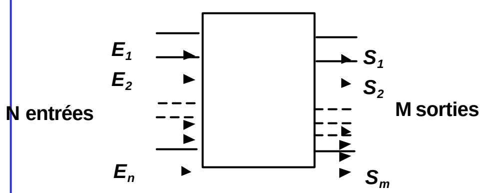
Circuits combinatoires

NON, ET, OU, OU Exclusif, …

Sortie(V,W,X,..) = f(A,B,C,…)

Pas de dépendance de l'état antérieur
=
Pas de dépendance du temps

Circuit combinatoire



Tout système combinatoire binaire peut être décomposé en fonctions ET, OU, NON

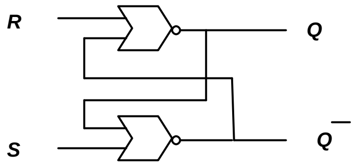
Circuit combinatoire

Tout système combinatoire binaire peut être décomposé en fonctions ET, OU, NON

—

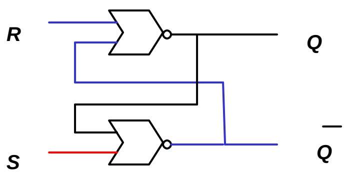
Réalisé avec des transistor MOS

Circuits séquentiels



Bascule RS

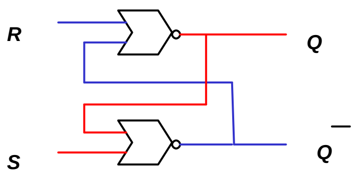
Bascule RS – Ecriture 1



S = 1 => $\bar{Q}$ = 0

R = 0

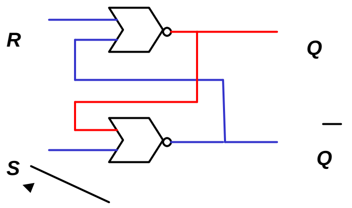
Bascule RS – Ecriture 2



S = 1 => Q = 1

R = 0

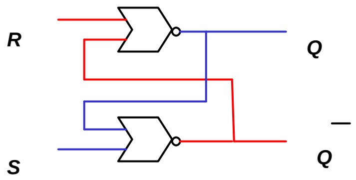
Bascule RS – Mémorisation



Changement d'état ne modifie pas la sortie

= Mémorisation du passage à 1

Bascule RS – Effacement



S = 0 => Q = 0

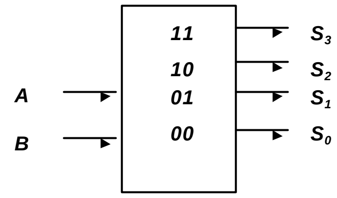
R = 1

Circuits séquentiels

Sortie(V,W,X,..) = f(A,B,C,…, états antérieurs)

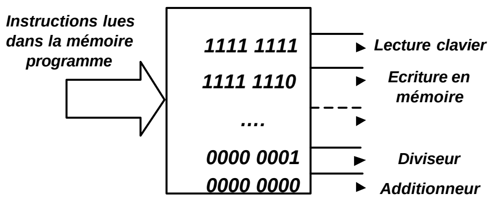
Dépendance des états antérieurs
=
Dépendance du temps

Circuits logiques



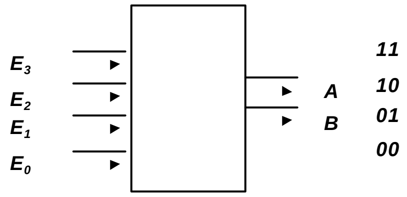
Décodeur

Circuits logiques



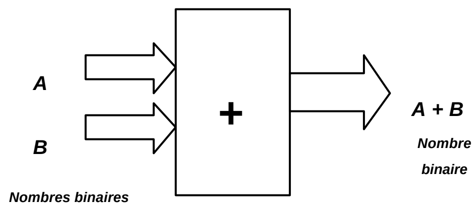
Décodeur d'instructions

Circuits logiques



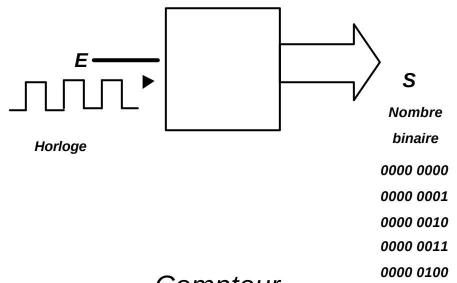
Encodeur

Circuits logiques



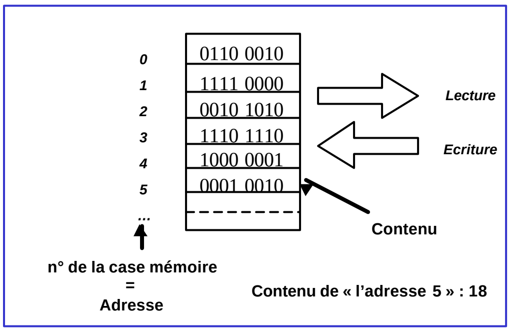
Additionneur

Circuits logiques

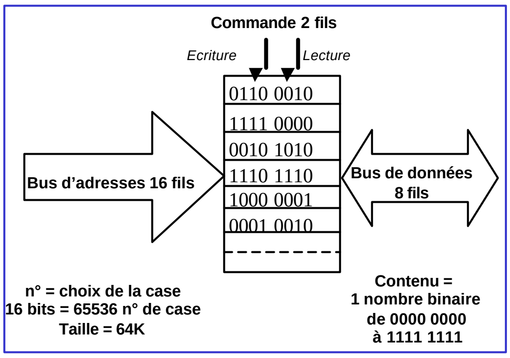


Compteur

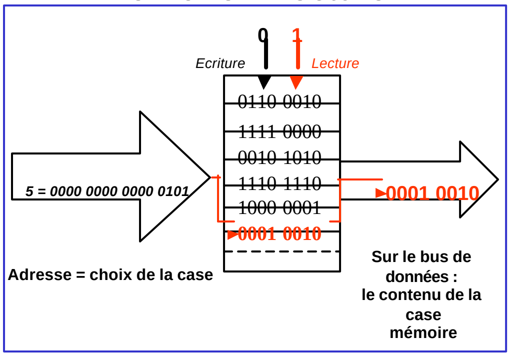
Mémoire



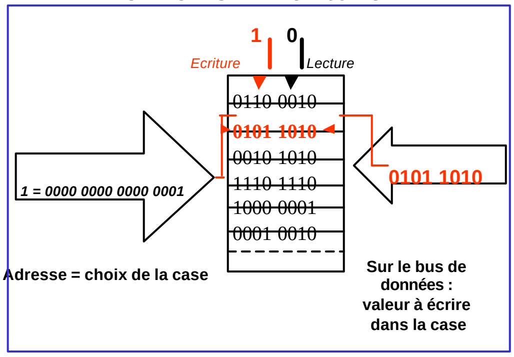
Mémoire - Fonctionnement



Mémoire - Lecture



Mémoire - Ecriture



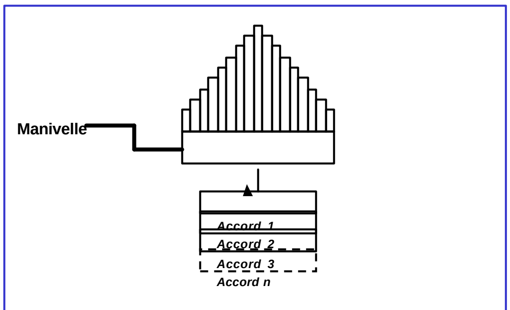
Chapitre 7

Système programmable

et

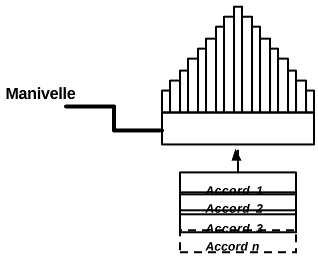
microprocesseur

Systèmes programmables



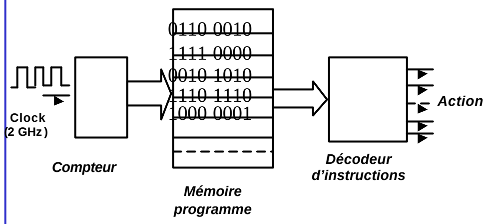
Orgue de Barbarie

Systèmes programmables



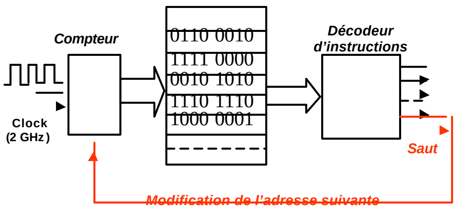
Orgue de Barbarie

Systèmes programmables



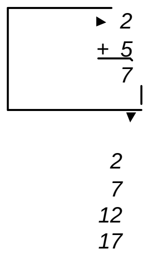
Système programmable
simple

Systèmes programmables



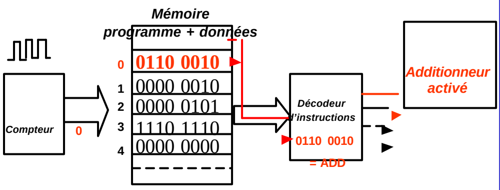
Système programmable avec saut

Machine von Neumann

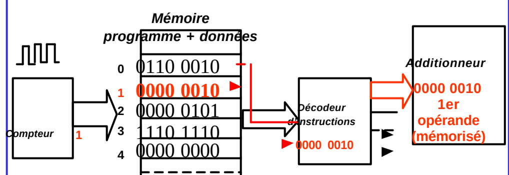


Calcul répétitif

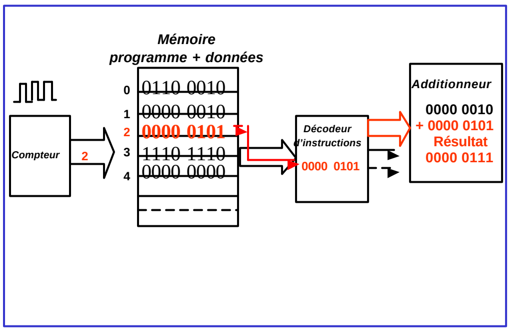
Machine von Neumann



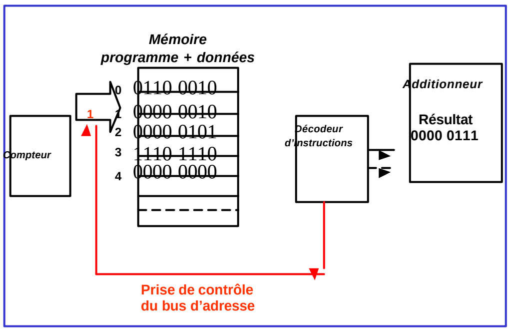
Machine von Neumann



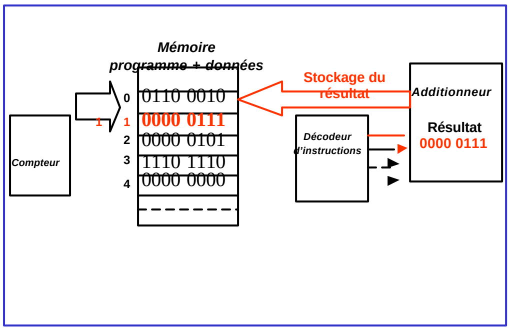
Machine von Neumann



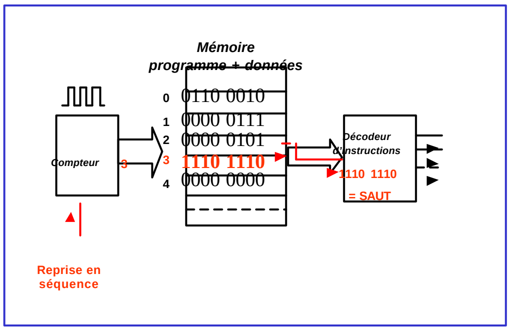
Machine von Neumann



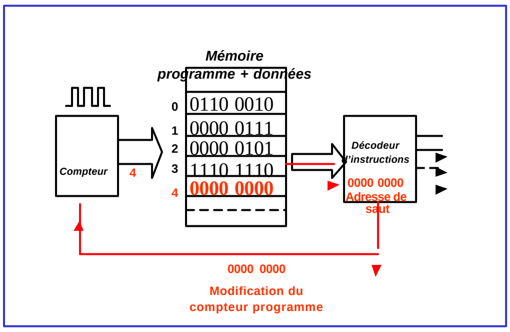
Machine von Neumann



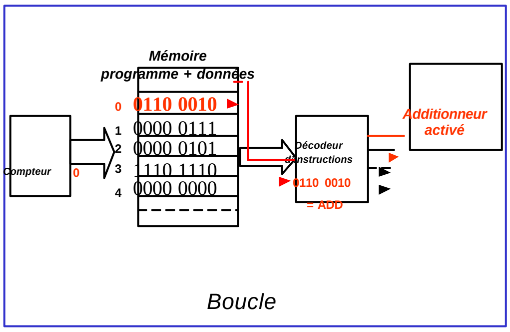
Machine von Neumann



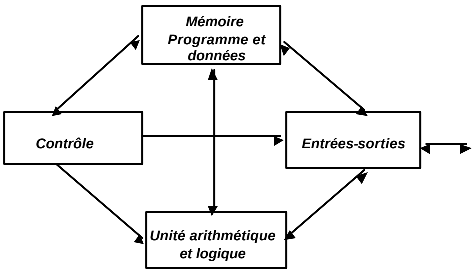
Machine von Neumann



Machine von Neumann



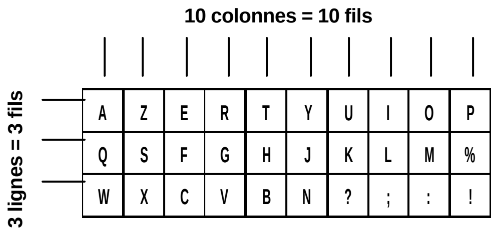
Architecture von Neumann



Chapitre 8

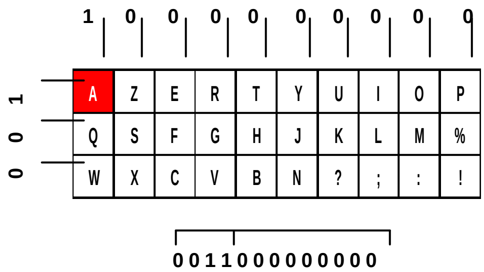
Du clavier à l'écran

Du clavier à l'écran

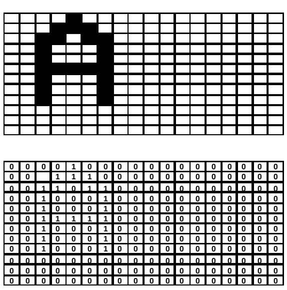


Clavier simplifié

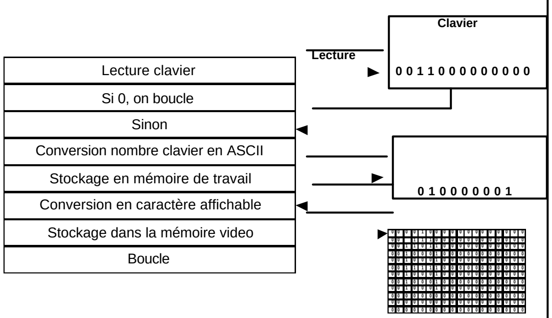
Du clavier à l'écran



Du clavier à l'écran



Du clavier à l'écran



Avantages du transistor MOS

TAILLE

Etching 0,1 µm => longueur = 0,4 µm

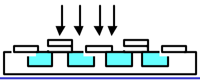
largeur = 0,1 µm

surface = 0,04 µm²

densité = 25 millions par mm²

1 transistor

4 x 0,1 µm



Avantages du transistor MOS

COMPLEXITE

CPU : 10 x 10 mm

Jusqu'à 2,5 milliards par puce

(500 millions en pratique)

FABRICATION

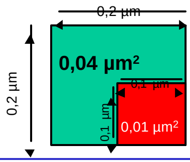
PLAN => facile par masques ou epitaxie

Avantages du transistor MOS

EVOLUTION

Etching / 2

⇒ Densité x 4



Avantages du transistor MOS

Evolution des processeurs Intel

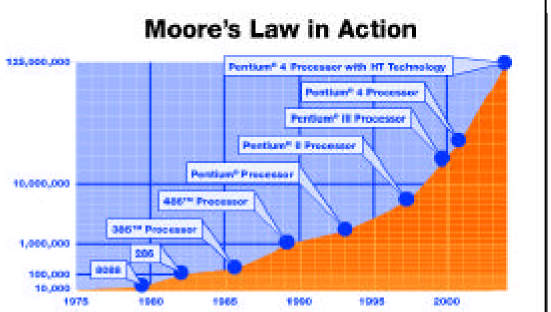
80386	1,5	µm
80486	1	µm
Pentium	0,7	µm
Pentium Pro	0,5	µm
Pentium II	0,35	µm
Pentium III	0,25	µm

Avantages du transistor MOS

Evolution des processeurs Intel

Pentium IV G1	0,18	µm
Pentium IV G2	0,13	µm
Pentium IV G3	0,1	µm
Itanium	0,07	µm

Avantages du transistor MOS



Comparaison avec la triode

CONSOMMATION

Consommation = 10^{-9} Watt

Rapport = $10^{-9}/20 = 5\ 10^{-11}$

1 / 20 Milliards

Comparaison avec la triode

MASSE

Masse = $4\ 10^{-11}\ cm^3 \times 4$ g

= $1{,}6\ 10^{-10}$ g

Rapport = $1{,}6\ 10^{-10}/100 = 1{,}6\ 10^{-12}$

1 / 600 Milliards

Comparaison avec la triode

VOLUME

Volume = $0{,}04\ \mu m^2 \times 1$ mm

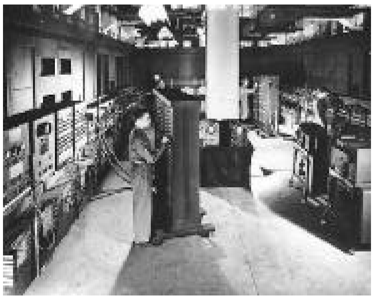
= $4\ 10^{-11}\ cm^3$

Rapport = $40\ 10^{-11}/40 = 10^{-12}$

1 / 1000 Milliards

ENIAC pesait 30 tonnes.

Disposé en une sorte de U
de 6 mètres de largeur
par 12 mètres de longueur



Elle consommait 200 kilowatts quand
elle était en marche

835 grammes